REMARKS

Claim 10 is currently amended. Claims 1-35 are pending in the application. Claims 1-6, 8-18, 20-28 and 30-35 are rejected. Claims 10 is objected to.

Claim Objections

Claim 10 was objected to for informalities. Claim 10 has not been substantively amended, but rather an inadvertent typographical error was corrected, which was inadvertently not corrected in the previous response, (*i.e.*, the spaces surrounding a previous amendment were underlined), in order to address the Examiner's objection. Applicant respectfully requests that the objection of claim 10 be withdrawn.

Allowable Subject Matter

Applicant acknowledges and appreciates that the Examiner has indicated that claims 7, 19 and 29 contain allowable subject matter.

Claim Rejection – 35 U.S.C. 112

The Examiner rejected claims 23-31 under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the enablement requirement. Applicant respectfully traverses this rejection.

In the Office Action, the Examiner argues that "the limitation 'A computer readable program' was claimed," but support for such a claim is not found in the Specification. *See* Office Action, p.3. Applicant respectfully submits that claim 23 does not simply recite a '[a] computer readable program' as alleged by the Examiner, but actually recites an apparatus in compliance with patentable statutory requirements. 35 U.S.C. §101. Applicants respectfully point out that the preamble of claim 23, read in proper context and in its entirety does not merely recite a "computer readable program," but goes further and actually recites "[a] **computer**

readable program storage device encoded with instructions." Bearing this in mind, the Specification offers exemplary embodiments of "a computer readable program storage device" which may be "encoded with instructions." For example, the Specification, Figures 2 & 3, show Memory Circuitry 250, as examples. Memory circuitry, as known by one of skill in the art, is computer readable, is able to store programs, and is able to be encoded with instructions. Additionally, the Specification also discloses computer components capable of supporting the claim 23 language" "[T]he software must run to receive and process data packets, the processor, memory, and other major components of the computer, cannot be placed into a true low-power mode." Specification, p.4, ll. 8-10 (*emphasis added*). The Specification further describes memory, in exemplary embodiments, at Specification, page 8, lines 8-21.

Moreover, the Specification indicates that the data detector/decoder 130 may take on various forms that are known to those skilled the art having benefit of the present disclosure. For example, the Specification discloses that the data detector/decoder 130 may be an integrated chip that contains **programmable** logic. Specification, p. 9, ll. 8-19. Those skilled in the art would understand that the term "programmable" refers to a computer readable program storage device that may be encoded with instructions. The programmable logic described in the Specification may be encoded with computer readable instructions to perform various functions. Those skilled in the art would understand that the disclosure with regard to the "programmable" logic clearly conveys an apparatus that may include a computer readable program storage device that may be encoded with instructions, which may be **programmed** to perform various method steps. Examples of such a device, as exemplified in the Specification, includes a "programmable logic chip," an "ASIC (application specific integrated circuit), etc. *See* Specification, p. 9, ll. 11-14. Therefore, in light of the various exemplary disclosures from the Specification provided above, it

is abundantly clear that those skilled in the art would readily find support for the "computer readable program storage device encoded with instructions," recited in claims 23-31.

For at least these reasons, the language "a computer readable program storage device encoded with instructions" is fully supported and enabled by the Specification. Applicant respectfully requests the rejections under 35 U.S.C. 112 be withdrawn.

Claim Rejection – 35 U.S.C. 103

In the present Office Action, the Examiner rejected claims 1-2, 9, 23-24, 31-32 and 34 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,802,305 ***(McKaughan)*** in view of U.S. Patent No 5,511,173 ***(Yamaura)***. Applicant respectfully traverses this rejection.

For ease of illustration, claim 1 is discussed first. Claim 1, directed to a method, calls for, among other things, detecting a size of said received set of data signals to use as a factor for decoding said data and decoding said received set of data signals.

The Examiner's rejection of claim 1 is incorrect at least because ***McKaughan*** and ***Yamaura***, either alone or in combination, do not teach or suggest all the claimed features. For example, claim 1 calls for detecting a size of said received set of data signals to use as a factor for decoding said data. In the Office Action dated December 30, 2009 [*hereinafter* Current Office Action], the Examiner admits that ***McKaughan*** does not teach this claimed feature. *See* Current Office Action, p.4. The Examiner, however, argues that ***Yamaura*** teaches this claimed feature, however, the Examiner offers no explanation or arguments in support of this conclusory assertion. *See id.* The Examiner cites to ***Yamaura***, col. 10, lines 24-29 in support of this rejection. This passage in ***Yamaura*** describes an instruction predecoder 33 which "predecodes the instruction and generates the corresponding control signal" and "supports the decoding operation in order to reduce the size of the [programmable logic array] PLA." *See* ***Yamaura***,

col. 10, lines 19-26. The cited passage in ***Yamaura*** further describes that the instruction predecoder 33 "includes the procedures for detecting the abbreviated instruction and the data size handled by the instruction." *See* ***Yamaura***, col. 10, lines 27-29. Thus, it is clear from the disclosure of ***Yamaura*** that the predecoder 33 it describes is used to help convert instructions that will be programmed into the PLA and to do so in a way that minimizes the *size of the PLA*. Put another way, the instruction predecoder 33 of ***Yamaura*** will simply decode the instructions **regardless** of the size of the received instruction, which is inapposite to the claims.

Indeed, a proper reading of ***Yamaura*** reveals that "detecting the abbreviated instruction and the data size handled by the instruction" is, in terms of decoding, agnostic with respect to "the data size handled by the instruction." *See* ***Yamaura***, Figs. 2A-2C and accompanying description at col. 3, line 64 to col. 4, line 39; col. 10, lines 27-29. Simply put, the decoding described in ***Yamaura*** involves "predecoding" a one-byte *abbreviated* operation code so a CPU can properly schedule execution of the operation. *See id.* The operation code is **not** dependent on the operand size. Thus, the instruction predecoder 33 **does not** rely upon detecting a size of said received set of data signals to use as a factor for decoding said data, as recited in claim 1, the instruction predecoder 33 will decode operation codes regardless of operand size.

As such, ***Yamaura*** does not teach detecting a size of the received set of data signals to use as a factor for decoding said data. Moreover, ***McKaughan*** fails to remedy this deficiency in ***Yamaura***, as admitted by the Examiner.

For at least the aforementioned reasons, claim 1 and its dependent claims are allowable. For at least similar reasons, claims 23, 32, and 34 (and their respective dependent claims) are also allowable.

Further, without using improper hindsight reasoning, those skilled in the art would not combine ***Yamaura*** and ***McKaughan*** in such a manner as claimed by the present application. Applicants respectfully assert that ***McKaughan***, ***Yamaura***, and/or their combination do not teach or disclose all of the elements of claims 1, 23, 32, and 34 of the present invention. In order to establish a prima facie case of obviousness, the Examiner must consider the following factors: 1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the teachings; 2) there must be a reasonable expectation of success; and 3) the prior art reference(s) must teach or suggest all the claim limitations. MPEP § 2143 (2005) (citing *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). In making an obviousness rejection, it is necessary for the Examiner to identify the reason why a person of ordinary skill in the art would have combined the prior art references in the manner set forth in the claims. *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007). Applicants respectfully submit that the Examiner has not met this burden. If fact, as illustrated herein, ***McKaughan*** and ***Yamaura*** are incompatible, and consequently those skilled in art would not combine them and make all of the elements of claims of the present invention obvious. Accordingly, Applicants respectfully submit that a *prima facie* case of obviousness has not been established in rejecting claims 1-2, 9, 23-24, 31-32 and 34.

McKaughan refers to a computer network that contains a plurality of interconnected computers, wherein a network interface card of sleeping computers detects an incoming packet and compares the incoming packet to a list of packets stored on the network interface cards. In contrast ***Yamaura*** is directed to effective minimization of PLA size and operation. ***Yamaura*** does not even mention the terms computer network, sleep or sleep mode. The Examiner uses

improper hindsight reasoning to combine ***McKaughan*** and ***Yamaura*** in the manner set forth in the claims. Further, the Examiner failed to identify any reason why those skilled in the art would combine ***McKaughan*** and ***Yamaura*** in the manner set forth in the claims. *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007). As such, the Examiner failed to establish a *prima facie* case of obviousness has not been established in rejecting claims 1-2, 9, 23-24, 31-32 and 34.

Without using improper hindsight reasoning and using the claim as a roadmap, the person of ordinary skill in the art would have no apparent reason to modify the references to arrive at the subject matter of claim 1. The Examiner essentially provided a **conclusory** statement that adding the features of these references together would make for a better product; *i.e.*, the Examiner has simply stated the result of such a combination. Indeed, the Examiner has offered **no motivation to combine whatsoever**. *See* Final Office Action, p.4-5 (stating "One skilled in the art would have recognized the detecting a size of said received set of data signals, and would have applied Yamaura et al.'s predecoder 33 in McKaughan et al.'s detects an incoming packet over the network."). As such, the Examiner has merely stated that such a combination would have been obvious. Such a statement is **purely conclusory** and insufficient in supporting a *prima facie* case of obviousness. However, the Examiner has not pointed to **any teachings** in the cited references that would **motivate** a person of skill in the art to combine the references. In other words, the question that must be addressed includes "***why*** would a person have thought to combine the cited references based on their teachings?", and "***what*** was the need?", not simply "what benefits would result?". Motivation to combine aside, as discussed above, even if ***McKaughan*** and ***Yamaura*** were to be combined, claim 1 as a whole would be untaught and non-obvious over the references. Therefore, claims 1-2, 9, 23-24, 31-32 and 34 are allowable for at least the reasons cited herein.

Additionally, claims 3-6, 8, 10-18, 20-22, 25-28, 30, 33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***McKaughan***, in view of ***Yamaura*** and further in view of U.S. patent No. 4,516,201 ***(Warren)***. Applicant respectfully traverses this rejection.

To the extent the Examiner relies upon ***McKaughan***, in view of ***Yamaura*** to reject claims 1-2, 9, 23-24, 31-32 and 34, Applicant has pointed out that ***McKaughan*** and ***Yamaura***, either alone or in combination, do not teach all the claimed features of claims 1-2, 9, 23-24, 31-32 and 34, nor would a person of skill in the art have been motivated to combine these references. Further, ***Warren*** fails to make up for these deficiencies; ***Warren*** is concerned with evenly managing data flow in a data link. As such, claims 3-6, 8, 25-28, 30, 33 and 35, which depend from claims 1, 23, 32 and 34, are allowable due at least to the nature of their respective dependencies.

With respect to claim 10, Applicant respectfully submits that all claimed features of claim 10 are not taught by ***McKaughan*** and ***Yamaura***, either alone or in combination, for at least similar reasons as argued above with respect to claim 1. ***Warren*** fails to make up for the deficiencies found in ***McKaughan*** and ***Yamaura***, for example, at least because ***Warren*** is concerned with evenly managing data flow in a data link and is silent with respect to <u>said decoded address data being based upon a content of said data signal and said size of said received data signals</u>. For at least these reasons, claim 10 (and its dependent claims) are also allowable.

For at least the reasons cite above, combining ***Warren***, with the disclosure of ***Yamaura*** and/or ***McKaughan***, would still not result in disclosing or making obvious all of the elements of any of the claims of the present invention. Therefore, claims 3-6, 8, 10-18, 20-22, 25-28, 30, 33, and 35, are not taught, disclosed, or made obvious by ***McKaughan***, ***Yamaura***, ***Warren***, or any

combination thereof. Accordingly, claims 3-6, 8, 10-18, 20-22, 25-28, 30, 33, and 35 are allowable for at least the reasons cited herein.

Applicant respectfully asserts that in light of the amendments and arguments provided by Applicant throughout the prosecution of the present application, all claims of the present application are now allowable and, therefore, request that a Notice of Allowance be issued.

Reconsideration of the present application is respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the **Examiner is respectfully requested to call the undersigned attorney** at the Houston, Texas telephone number (713) 934-4069 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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Date: March 30, 2010

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